AMENDMENTS TO THE CLAIMS

Please amend the claims as follows (with strikethrough indicating deletions and underlining indicating additions to the amended claims):

1. (Currently Amended) A method for storing an incoming datagram in a switch matrix of a switch fabric, the switch matrix having a pair of buffers, each buffer having a pair of portions, comprising:

(a) receiving data of a datagram utilizing an interface receiver, wherein the pair of buffers are uniquely associated with the interface receiver to receive only data from an incoming datagram received by the interface receiver;

(b) sequentially filling the buffer portions with the data of the datagram, wherein each buffer has a storage capacity less than the size of the incoming datagram;

(c) periodically allowing transfer of data from the buffers into the switch matrix; and

(d) transferring the data in one of the buffer portions into the switch matrix at each period where transfer of data is allowed and in the sequence that the buffer portions were filled.

2. (Original) The method of claim 1, wherein data in a buffer portion can only be transferred into the switch matrix if the buffer portion is filled with data or contains an end of a datagram.

3. (Original) The method of claim 1, wherein the switch matrix comprises a plurality of memory banks for storing the transferred data.

4. (Original) The method of claim 3, wherein the memory banks alternate in receiving data transferred from the buffer portions.

5. (Original) The method of claim 1, wherein the buffer portions each have equal storage capacities.

6. (Original) The method of claim 5, wherein each buffer portion has a storage capacity of 16 bytes.

7. (Original) The method of claim 1, wherein transfer of data is allowed every 16 cycles.

8. (Currently Amended) A system for storing an incoming datagram in a switch fabric, comprising:

at least one interface receiver adapted for receiving data of an incoming datagram;

a switch matrix having a pair of buffers for each interface receiver, each pair of buffers being uniquely associated with its respective interface receiver to receive data from an incoming datagram received by its associated interface receiver, each buffer having a pair of portions in communication with the interface receiver to permit sequentially filling of the buffer portions with the data of the incoming datagram, wherein each buffer has a storage capacity less than the size of the incoming datagram;

the switch matrix having a memory in communication with the buffer portions; and

control logic for periodically allowing transfer of data from the buffers into the memory, wherein data in one of the buffer portions is transferred into the switch matrix at each period where transfer of data is allowed and in the sequence that the buffer portions were filled.

9. (Original) The system of claim 8, wherein data in a buffer portion can only be transferred into the switch matrix if the buffer portion is filled with data or contains an end of a datagram.

10. (Original) The system of claim 8, wherein the memory comprises a plurality of memory banks each adapted for storing the transferred data.

11. (Original) The system of claim 10, wherein the memory banks alternate in receiving data transferred from the buffer portions.

12. (Original) The method of claim 8, wherein the buffer portions each have equal storage capacities.

13. (Original) The method of claim 12, wherein each buffer portion has a storage capacity of 16 bytes.

14. (Original) The method of claim 8, wherein transfer of data is allowed every 16 cycles.

15. (Currently Amended) A computer program product for storing an incoming datagram in a switch matrix of a switch fabric, the switch matrix having a pair of buffers, each buffer having a pair of portions, comprising:

(a) computer code for receiving data of a datagram utilizing an interface receiver, wherein the pair of buffers are uniquely associated with the interface receiver to receive only data from an incoming datagram received by the interface receiver;

(b) computer code for sequentially filling the buffer portions with the data of the datagram, wherein each buffer has a storage capacity less than the size of the incoming datagram;

(c) computer code for periodically allowing transfer of data from the buffers into the switch matrix; and

(d) computer code for transferring the data in one of the buffer portions into the switch matrix at each period where transfer of data is allowed and in the sequence that the buffer portions were filled.

16. (Original) The computer program product of claim 15, wherein data in a buffer portion can only be transferred into the switch matrix if the buffer portion is filled with data or contains an end of a datagram.

17. (Original) The computer program product of claim 15, wherein the switch matrix comprises a plurality of memory banks for storing the transferred data.

18. (Original) The computer program product of claim 17, wherein the memory banks alternate in receiving data transferred from the buffer portions.

19. (Original) The computer program product of claim 15, wherein the buffer portions each have equal storage capacities.

20. (Original) The computer program product of claim 15, wherein transfer of data is allowed every 16 cycles.

Please add the following new claims.

21. (New) A method for storing an incoming datagram in a switch matrix of a switch fabric, the switch matrix having a pair of buffers uniquely associated with an ingress receiver, each buffer having a pair of portions, comprising:

(a) receiving data of a datagram utilizing the ingress receiver;

(b) sequentially filling the buffer portions associated with the ingress receiver with the data of the datagram, wherein the buffer portions have equal storage capacities, wherein the incoming datagram has a length greater than the storage capacity of either buffer;

(c) periodically allowing transfer of data from the buffers into the switch matrix, wherein the switch matrix comprises a plurality of memory banks for storing the transferred data; and

(d) transferring the data in one of the buffer portions into the switch matrix at each period where transfer of data is allowed and in the sequence that the buffer portions were filled, wherein data in a buffer portion can only be transferred into the switch matrix if the buffer portion is filled with data or contains an end of a datagram, wherein the memory banks alternate in receiving data transferred from the buffer portions.